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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,993	08/09/2001	Harsh D. Sharma	SP-6183 US	4755

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EXAMINER	
LUGO, DAVID B	
ART UNIT	**PAPER NUMBER**
2637	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/925,993	SHARMA ET AL.	
	Examiner	Art Unit	
	David B. Lugo	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Page 7, line 1, "value 517" and "value 515" should be --value 617-- and --value 615--, respectively, to correspond with Fig. 6.

Appropriate correction is required.

Claim Objections

2. Claims 9 and 10 are objected to because of the following informalities:

Claim 9, line 3, it is suggested that "the first adjacent signal" be amended to --the second adjacent signal--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durham et al. U.S. Patent 6,532,574 in view of Cai et al. U.S. Patent Application Publication 2002/0124230.

5. Regarding claims 1 and 13, Durham et al. disclose a method for transmitting signals in an integrated circuit where the timing of a signal line selected from a pair of adjacent signal lines (step 706) is altered (step 710) by delaying the edge of the clock signal for the logic driving the selected signal line in order to reduce noise-induced delay variations (col. 8, lines 24-33).

6. Durham et al. does not disclose the criteria used for determining which signal line is selected.

7. Cai et al. disclose a timing optimization method where signal paths are assigned priority in order of greatest delay to least delay (page 5, paragraph 56).

8. It would have been obvious to one of ordinary skill in the art to use the priority scheme of Cai et al. to determine the signal line to be selected for being delayed in the method of Durham et al. in order to optimize timing by preventing the signals with the longest delays from being delayed further.

9. Regarding claims 2 and 14, the delay is a pulse signal (delay_rise – Fig. 4) transmitted to the selected adjacent signal for altering the edge of the clock for the logic driving the signal line.

10. Regarding claims 3 and 15, Durham et al. state that steps 706 and 710 are repeated, where a delay for a second signal adjacent to the signal of the original signal pair that is not delayed may be provided (col. 8, lines 33-40).

11. Regarding claims 4 and 16, the delays are pulse signals (delay_rise – Fig. 4) transmitted to the adjacent signals for altering the edge of the clocks for the logic driving the signal lines.

12. Regarding claims 5 and 17, Durham et al. state that steps 706 and 710 are repeated, where a delay for additional signals are provided (col. 8, lines 33-40).

13. Regarding claims 6 and 18, the delay is a pulse signal (delay_rise – Fig. 4) transmitted to a selected adjacent signal.

14. Regarding claim 7, Durham et al. disclose an integrated circuit where a delay signal is provided to a signal driver, where the timing of a signal line selected from a pair of adjacent signal lines (step 706) is altered (step 710) by delaying the edge of the clock signal for the logic

driving the selected signal line in order to reduce noise-induced delay variations (col. 8, lines 24-33, Fig. 6, claim 15).

15. Durham et al. do not disclose priority signals for determining which signal line is selected.

16. Cai et al. disclose a timing optimization method where signal paths are assigned priority in order of greatest delay to least delay (page 5, para. 56).

17. It would have been obvious to one of ordinary skill in the art to use priority signals as taught by Cai et al. to determine the signal line to be selected for being delayed in the method of Durham et al. in order to optimize timing by preventing the signals with the longest delays from being delayed further.

18. Regarding claim 8, the delay is a pulse signal (delay_rise – Fig. 4) transmitted to the selected adjacent signal for altering the edge of the clock for the logic driving the signal line.

19. Regarding claim 9, Durham et al. state that steps 706 and 710 are repeated, where a delay for a second signal adjacent to the signal of the original signal pair that is not delayed may be provided (col. 8, lines 33-40).

20. Regarding claim 10, the delays are pulse signals (delay_rise – Fig. 4) transmitted to the adjacent signals for altering the edge of the clocks for the logic driving the signal lines.

21. Regarding claim 11, Durham et al. state that steps 706 and 710 are repeated, where a delay for additional signals are provided (col. 8, lines 33-40).

22. Regarding claim 12, the signal driver is part of an integrated circuit (see abstract).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David B. Lugo whose telephone number is 571-272-3043. The examiner can normally be reached on M-F; 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

dl
12/17/04

KEVIN BURD
PRIMARY EXAMINER